# *METS*: A *M*etric for *E*lectro-*T*hermal *S*ensitivity, and Its Application To FinFETs

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## Abstract

*While device dimensions continue to shrink into the sub-90nm range, device self-heating emerges as a pressing problem, affecting both mobility and leakage current. Coupled electro-thermal simulation can be used to assess the impact. Simulation, however, is time consuming. Furthermore, it does not give insight into the device's performance robustness against self-heating.*

*We propose in this paper a novel metric,* M*etric for* E*lectro-*T*hermal* S*ensitivity (METS), for characterizing a device's electrical robustness to self-heating. We demonstrate the effectiveness of METS in characterizing FinFETs, novel double-gate devices promising to replace traditional MOSFETs because of their reduced leakage currents. FinFETs are an ideal case study for METS as they have ultra thin bodies and are thus prone to self-heating. We show that our proposed metric, METS, is capable of characterizing the self-heating behavior of FinFETs in the On and Off states.*

## 1. Introduction

Next-generation VLSI circuits will be composed of devices with dimensions in the nanometer range (e.g. sub-100nm gate lengths). The 2003 International Technology Roadmap for Semiconductors predicts several transistor improvements, including strained Si-channels, ultra-thin bodies, and metallic junctions [6]. It also predicts the move towards double-gate devices which allow more than one gate terminal to control the transistor channel.

The complex and confined geometries of future devices causes significant self-heating. The resulting thermal impact can be detrimental for performance. For example, Jenkins and Franch recently investigated how self heating in SOI CMOS circuits affects worst-case drain current [7]. They showed how localized temperature differences due to internal and coupled heating can generate drain current mismatch.

With the potential impact of temperature on performance, thermal device design becomes important especially for analog circuits. In thermal device design, the goal is to maximize device thermal robustness under process and operating variations, while meeting performance and reliability requirements. Thermal simulation techniques for nanoscale transistors thus become important.

Thermal simulation techniques have evolved in the past decade. Earlier efforts focused on simulating heat generation through a solution of Fourier's Law, the classical heat diffusion equation. Device thermal modeling consisted of modeling a device as a transient three-dimensional heat flow problem [8, 20]. The temperature at any point within the device can be found at any instant in time. The heat diffusion equation however fails to capture the dominant thermal energy transport mechanism due to phonons, particles that transport energy, and atomic lattice vibrations. Monte Carlo simulation methods can be used to compute detailed phonon generation rates at various electric fields in doped bulk and strained silicon devices [17]. The shrinking nanoscale transistors, however, exhibit nearly ballistic transport for both electrons and phonons. Recently, the Boltzmann Transport Equation (BTE) was used to estimate the hot spots associated with the drain regions [23, 15]. Sverdrup, Ju, and Goodson compared the BTE to classic heat diffusion temperature estimations within a MOSFET device. They found the heat diffusion equation underestimates the maximum device temperature, when compared to BTE estimates, by as much as 159% [23]. The BTE can be solved for both electrons and phonons, and the results can be coupled together allowing for accurate estimation of localized hot spots within a device [21].

We propose in our paper a novel metric for measuring device robustness to thermal effects. The metric, *METS* (*M*etric for *E*lectro-*T*hermal *S*ensitivity), ranges from 0 to 1. Unity indicates that the device's electric behavior is robust to device self-heating. As the metric value tends to zero,

the metric indicates that a device is prone to self-heating, resulting in significant changes in the device's electrical behavior. The metric is derived from electro-thermal device simulations. In such a simulation, tight interaction between the electrical and thermal device models dictate the final device current and temperature profile.

An electro-thermal sensitivity metric that characterizes self-heating must have the following characteristics:

- For the metric to be useful, it should not depend on a particular operating temperature. The metric should remove the impact of operating at a particular temperature.
- The metric should be able to capture the effects of device processing and geometries.
- The metric must be independent of the method used to obtain the underlying simulation results as we wish the metric to remain valid with advances in simulation and modeling technologies.
- It is desirable that the metric is general and can be applied to a wide range of devices, thus allowing useful comparisons about device sensitivities in different regions of operation.

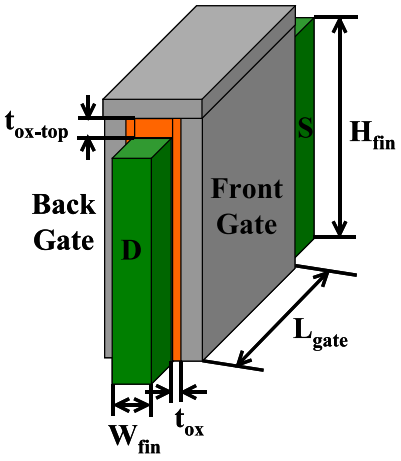



**Figure 1.** FinFET device.

To illustrate the utility of our metric, *METS*, we use it to evaluate the robustness of FinFET devices. A FinFET is a quasi-planar double-gated device where a silicon fin protrudes out of the surface of the silicon wafer. The FinFET is formed by draping a gate atop the fin and doping the ends of the fin to form the source and drain (see Figure 1). FinFETs, originally dubbed as the folded-channel MOSFET [5], show high current drive and offer substantially better control over leakage and short channel effects when compared to traditional MOSFETs. Among double-gated devices, FinFETs are more promising because of their self-aligned front and back gates.

The FinFETs form the quintessential case study of our metric. They provide excellent electrostatic characteristics, but suffer from significant self-heating. SOI FinFETs are more susceptible to self-heating than bulk devices: SOI thermal conductivity is two orders of magnitude less than that of silicon [22]. Furthermore, the small and confined dimensions of the fin reduce the thermal conductivity (which increases the thermal resistance) of the device due to reduced phonon mean path [9]. Heat transport out of the device is hindered, and the device temperature rises. Careful device thermal analysis is needed to balance the device's electrical characteristics with thermal ones [2]. FinFET thermal problems are further exasperated with the construction of wider FinFETs built using parallel fins between the source and the drain areas. These fins are tightly laid out causing heat to spread among the fins.

We begin our paper with an overview of the electro-thermal modeling of FinFETs and our SPICE modifications to co-simulate the electrical FinFET properties coupled with the thermal equivalent network. We then introduce our metric. Next, we evaluate the metric for FinFETs operating in the on and off regions. We conclude with future research directions that highlight the role of thermal device modeling and its implication on circuit design.

## 2. Electro-Thermal Modeling of FinFETs

A detailed discussion of heat generation within transistors can be found in [11, 18]. For FinFET thermal modeling, we adopt Pop et al.'s thermal model for an ultra-thin body SOI (UTB-SOI) device [16]. The model uses a reduced thermal conductivity factor to account for the thin device geometry and impurity effects on the phonon mean free path. While not accounting for all thermal nano concerns, the model is reasonably applicable for FinFETs, and for the purposes of illustrating the application of METS.

An ultra thin device and its equivalent UTB model are respectively shown in Figure 2 and in Figure 3 (right circuit). The gate, drain, and source pads are assumed to connect through metal contacts to other circuit elements. Their top surface is assumed to be at a reference temperature. Adiabatic boundary conditions are applied to all other surfaces. Thus heat only flows in and out of the device at the top surface of the pads. Equivalent thermal resistances are calculated using the thermal resistance equation for rectangular shapes: $R = L/kA$, where $L$ is the length of the rectangle, $A$ is the cross sectional area, and $k$ is the thermal conductivity. The current source representing the heat $Q$ can be applied to the UTB model at the drain node since it is the heat generation region. Thermal analysis (de-coupled of the electric network) can be done to this model as follows: The injected

current can be calculated using the dot product of the current density and the electric field within the device. Circuit analysis can then be used to solve for the temperatures at the drain, source, channel, and gate.

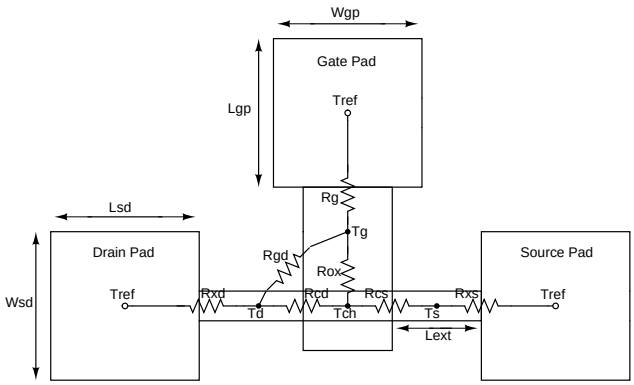



**Figure 2.** Top view of a FinFET layout with equivalent thermal resistances [16]. Only one gate pad is used for this analysis.

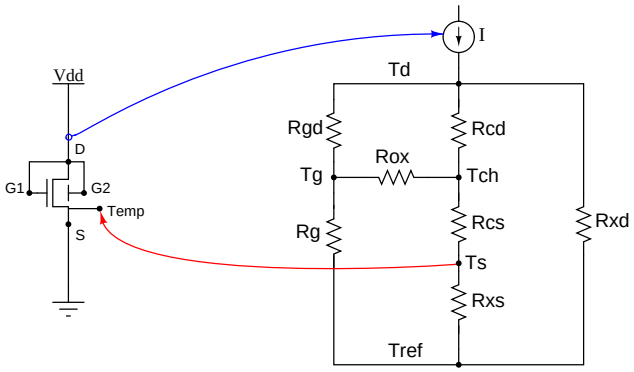



**Figure 3.** SPICE-based electro-thermal simulation. The FinFET electrical model is on the left is coupled with Pop's equivalent thermal model [16] on the right. The lower arrow indicates the dependence of the device current on the source temperature, and the upper arrow indicates the dependence of the temperature on the current flow in the device.

## 3. Electro-Thermal Simulation

Heat applied to the thermal circuit in Figure 3 is dependent on the current flowing through the device. However, the current flowing through the device is dependent on the device source temperature, due to the temperature dependence of mobility and threshold voltage [16, 13]. We establish coupled electrical/thermal simulation as shown in Figure 3.

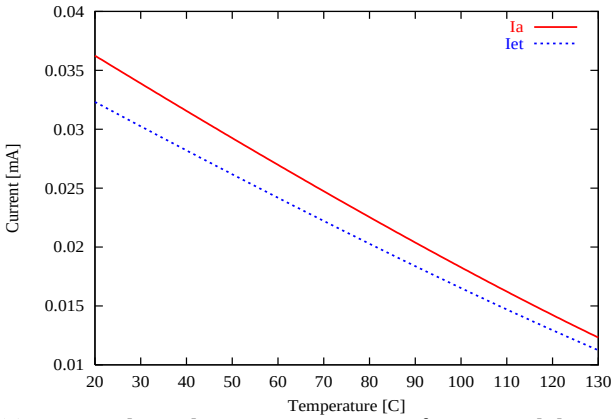
Our electro-thermal methodology uses the thermal circuit shown in Figure 3 and updates all electrical temperature sensitive parameters, mainly mobility and threshold voltage, at every transient time step in our modified version of SPICE. We couple the electrical and thermal circuits together through dependent sources, and then perform SPICE simulations. Our electro-thermal simulations allow us to simultaneously: (1) model the temperature effect within each fin on its current, and (2) model the effect of current change on the temperature of each fin. We thus produce accurate drain, gate, source, and channel temperature estimations for each fin.

Electro-thermal simulations have been studied over the past several decades, with numerous approaches. The majority of these works target full chip electro-thermal simulations, requiring reduced thermal networks and/or simplified electrical models [10, 4, 24, 19, 3, 26]. Unlike these target applications, we are interested in detailed device-level electro-thermal device analysis. We have borrowed previous electro-thermal analysis techniques from Liu et al. and Chiang et al. [12, 1]. Liu et al. constructed electro-thermal device models which are thermally compensated for self-heating by altering carrier mobility and threshold voltage using an RC equivalent thermal circuit. Chiang et al. used SPICE to solve a 3-D distributed thermal circuit model for interconnects. Their model accounts for interconnect self-heating and heat spreading to neighboring interconnects and layers.

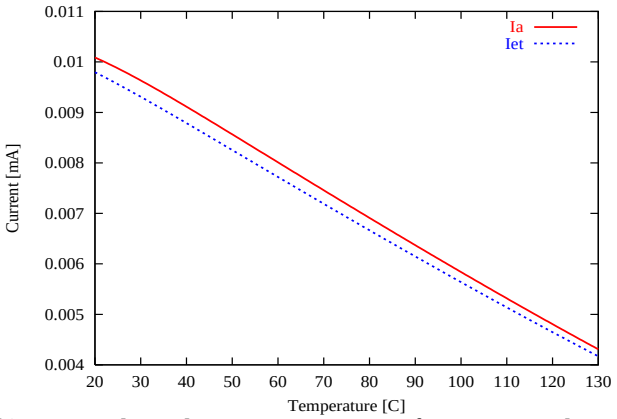
Electro-thermal simulation is essential in avoiding the overestimation of the maximum fin temperatures and in accurately estimating the current. Figure 4(a) illustrates the current in a FinFET device with and without electro-thermal simulations. $I_a$ is the current obtained by assuming that the fin temperature is the one given on the x-axis. $I_{et}$ is the current obtained using electro-thermal simulations where the ambient temperature was the one given on the x-axis. $I_{et}$ then reflects device self-heating as well as the ambient temperature. The figure illustrates the over-estimation of the current without using the electro-thermal simulation. At $20°C$, the difference between the two simulations is about 11%. The difference is smaller at higher temperatures.

## 4. *METS*: *M*etric for *E*lectro-*T*hermal *S*ensitivity

Contrasting electrical and electro-thermal simulations can evaluate the particular contribution of self-heating for a particular device at a specified temperature. That is, at a particular temperature in Figure 4(a), the difference between $I_a$ and $I_{et}$ is the degradation in current due to self-heating. Or equivalently, for a particular current value, the $\Delta x$ between $I_a$ and $I_{et}$ represents the effective change in temperature due to self-heating. For example, in Figure 4(a) a device oper-




(a) Current dependence on temperature for nominal device.




(b) Current dependence on temperature for 0.2x $W_{fin}$ device.

**Figure 4. Experimental data to illustrate current dependence on temperature.**

ating with a current of 0.03mA has an effective $\sim 15°C$ of self-heating.

To establish our metric, we utilize the difference between $I_a$ and $I_{et}$ at different temperatures. We characterize each simulation in Figure 4(a) by a sensitivity slope, $S_a$ or $S_{et}$, over a wide range of operation. The sensitivity slope reflects the change in current due to temperature changes. In the case of $S_a$, the slope captures changes in ambient temperature. For $S_{et}$, the slope captures temperature due to both self-heating and ambient temperature. We can then express our self-heating metric for a device as $S_{et}/S_a$. Our equations are summarized below:

$$\begin{aligned} S_{et} &= \frac{I_{et_{T_2}} - I_{et_{T_1}}}{T_2 - T_1} \\ S_a &= \frac{I_{a_{T_2}} - I_{a_{T_1}}}{T_2 - T_1} \\ METS &= S_{et}/S_a \end{aligned} \tag{1}$$

METS is confined to the range of [0,1]. A device with no self-heating will have $METS$ equal to one, that is, $I_a$ and $I_{et}$ will be parallel. However, a device with substantial self-heating will have a METS ratio less than one. Our nominal device simulated here as a METS ratio of 0.875.

## 5. Experimental Results

Figure 5 shows the METS ratio for a single-fin device with some geometric ($W_{fin}$, $H_{fin}$, $L_g$, $H_g$, and $T_{ox}$) variations. Our baseline (nominal) device is a single fin with the parameters shown in Table 1. Each point on the graph represents the METS for a given deviation from a nominal device, referred to as 1x.

From the METS plot, we can see that some variations in the device, such as $T_{ox}$ variations, contribute the least to self-heating effects. In contrast, any changes in $L_g$ results

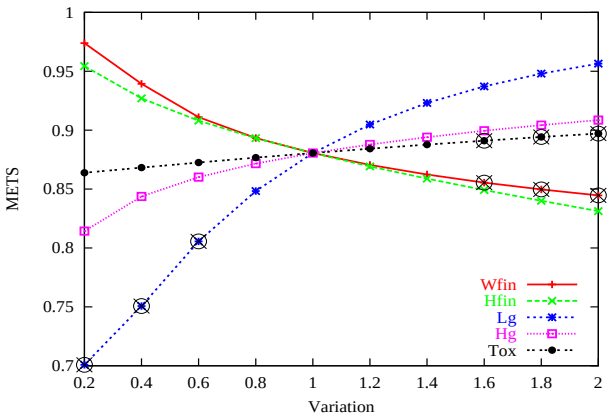



**Figure 5.** Thermal sensitivity plot for single-fi n device. The parameter variation ranges from 0.2x to 2x a nominal device.

in significant device self-heating. The circles with X's in them represent devices which do not meet recommended device geometries. For example, Gen et al. recommends the ratio: $W_{fin} \leq 0.5\ L_{eff} - 6\ t_{ox}$ for reduced DIBL and ideal subthreshold swing [14]. Yu et al. provides the ratio: $W_{fin} \leq 5\ L_{eff}$ for an acceptable fin aspect ratio [25]. The METS plot thus provides a good way of evaluating how the device self-heating will change under process variations.

Examining the $W_{fin}$ thermal sensitivity line in Figure 5 shows a thinner fin is more robust than a wider fin. For example, the thermal sensitivity of a 0.2x device is larger than the thermal sensitivity of a nominal device, thus the thinner fin is less sensitive to self-heating. This is justified when comparing the slopes of $I_a$ and $I_{et}$ in Figure 4(b) against the slopes of $I_a$ and $I_{et}$ in Figure 4(a). As Figure 4 shows, the slopes in (b) are almost parallel resulting in near ideal ther-

| $L_g$ | $H_g$ | $W_g$ | $H_{fin}$ | $W_{fin}$ | $t_{ox}$ | $L_{ext}$ | $L_q$ | $L_{sd}$ | $W_{sd}$ |
|---|---|---|---|---|---|---|---|---|---|
| $50nm$ | $75nm$ | $140nm$ | $65nm$ | $10nm$ | $16\AA$ | $50nm$ | $5nm$ | $200nm$ | $200nm$ |

| $H_{sd}$ | $L_{gp}$ | $W_{gp}$ | $W_{space}$ | $R_{if}$ | $k_g$ | $k_{ch}$ | $k_{ext}$ | $k_{ox}$ | $k_{sd}$ |
|---|---|---|---|---|---|---|---|---|---|
| $65nm$ | $200nm$ | $200nm$ | $100nm$ | $20E-9\frac{m^2 \cdot K}{W}$ | $45.3\frac{W}{m \cdot K}$ | $6.5\frac{W}{m \cdot K}$ | $13.0\frac{W}{m \cdot K}$ | $1.38\frac{W}{m \cdot K}$ | $13.0\frac{W}{m \cdot K}$ |

**Table 1.** Model FinFET dimensions and thermal conductivities

mal sensitivity and higher thermal sensitivity than in (a).

We expect the FinFETs to be robust to self-heating when the device is off because FinFETs have notably low leakage currents in the $100 - 500\,fA$ range. The low leakage current generates very little heat in the device, which causes negligible self-heating. This is reflected in the current as shown in Figure 6(a). The METS for the nominal FinFET and its deviations are shown in Figure 6(b), and as expected the METS for a device operating in an off state is unity.

## 6. Conclusion

We developed in this paper a metric, *METS*, for measuring electro-thermal device sensitivity. *METS* can be used to characterize device robustness against self-heating. We utilized reduced thermal conductivities from BTE results in our electro-thermal simulations to capture the sub-continuum effects of nanoscale devices. Our SPICE-based co-simulation methodology provides an easy way to accurately predict device temperatures and performance in FinFETs, and can be applied to other nanoscale devices.

This work is important as it is the first to characterize the impact of self-heating on circuit performance for FinFETs. Our findings motivate further research into the newly emerging area of research, *electro-thermal device design*, and how metrics such as METS can be used to optimize device design. Understanding thermal device sensitivities will help understand the impact of process variations, a critical challenge in 65nm and beyond designs.

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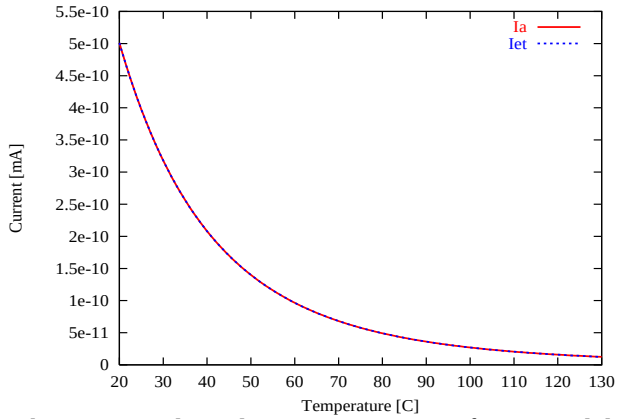
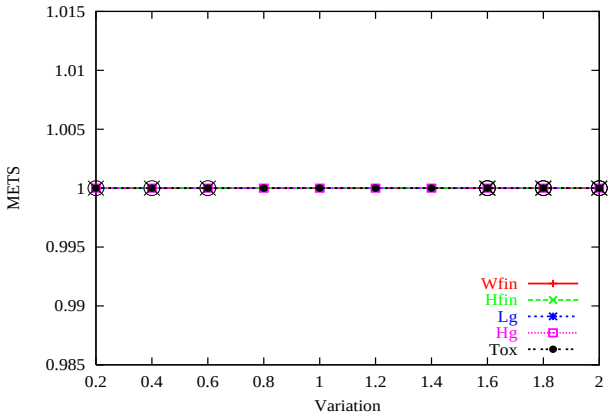



(a) Leakage current dependence on temperature for nominal device.




(b) METS for Off operation for the nominal FinFET.

**Figure 6. Experimental data to illustrate leakage current lack of dependence on temperature.**

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